CPU MF Formulas and Updates

April 2025

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Bradley Snyder

Document Contents

z/OS SMF 113 Record

SMF113_1_CTRVN2

- “1” = z10
- “2” = z196 / z114
- “3” = zEC12 / zBC12
- “4” = z13 / z13s
- “5” = z14
- “6” = z15
- “7” = z16
- “8” = z17

z/VM Monitor Domain 5 Record 13" and the field is "PRCMFC_CSVN"; same values and meaning as CTRVN2

L1MP and RNI-based LSPR Workload Decision Table

L1MP	RNI	LSPR Workload Match
< 3%	>= 0.75 < 0.75	AVERAGE LOW
3% to 6%	>1.0 0.6 to 1.0 < 0.6	HIGH AVERAGE LOW
> 6%	>= 0.75 < 0.75	HIGH AVERAGE

Current table applies to all IBM Z Processors from z10 through z17 CPU MF Data

*** Updated December 2024**

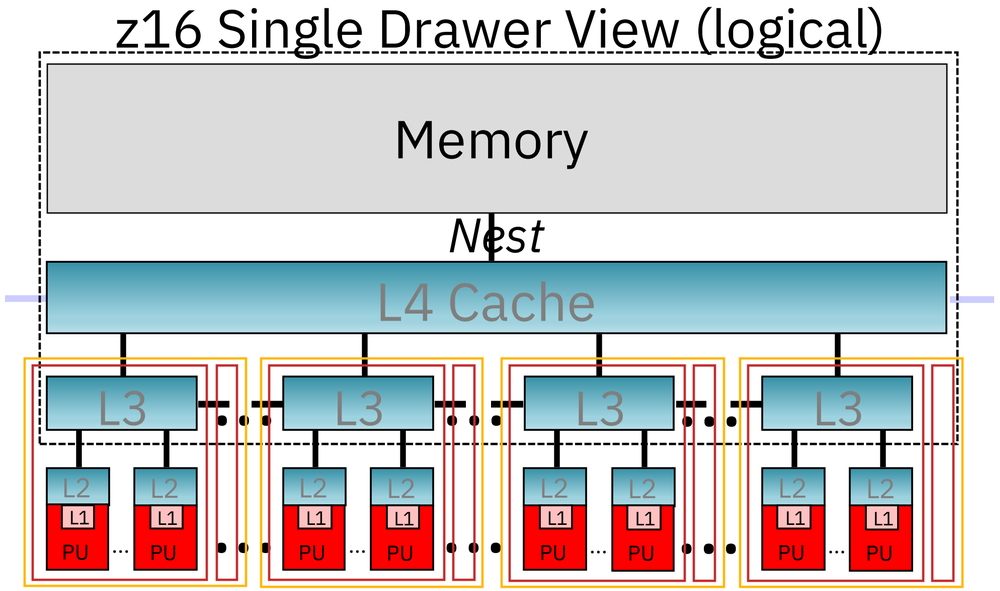
The LSPR Workload Match no longer considers zIIPs

IBM z17 Metrics

z17 vs z16 Hardware Comparison

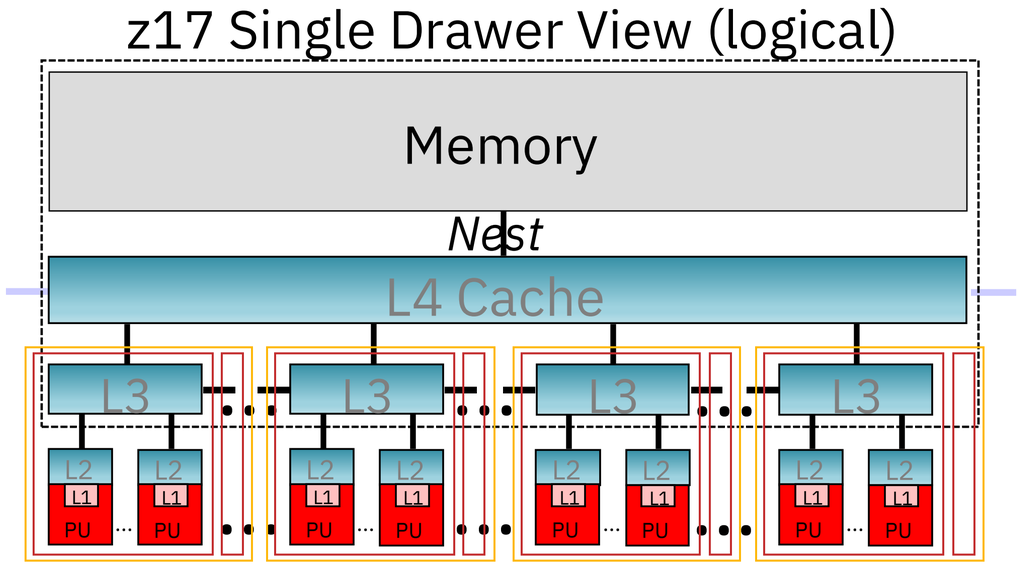
z16

CPU	5.2 GHz
Caches	L1 private 128k i, 128k d / core L2 *private* 32 MB unified / core virtual L3 up to 7x32 = 224 MB / CP chip virtual L4 up to 8x32x7 = 1.75 GB / drawer
Topology	8 (core + L3)s / CP chip 2 CP chips / DCM 4 DCMs (64 engines) / drawer 4 drawers / CEC Book interconnect: numa star



z17

CPU	5.5 GHz
Caches	L1 private 128k i, 128k d / core L2 private 36 MB unified / core virtual L3 shared up to 9x36 = 324 MB / CP chip virtual L4 shared up to 10x36x7 = 2.52 GB / drawer
Topology	8 (core + L3)s / CP chip 2 CP chips / DCM 4 DCMs (64 engines) / drawer 4 drawers / CEC Book interconnect: numa star



Formulas – z17

Updated April 8, 2025

Note these Formulas may change in the future

Metric	**Calculation –** *note all fields are deltas. SMF113-1s are deltas. SMF 113-2s are cumulative.*
CPI	B0 / B1
PRBSTATE	(P33 / B1) * 100
L1MP	((B2+B4) / B1) * 100
L2P	((E145+E146+E169+E170) / (B2+B4)) * 100
L3P	((E147+E149+E150+E151+E171+E173+E174+E175) / (B2+B4)) * 100
L4LP	((E148+E152+E153+E154+E160+E161+E162+E163+E164+E165+E172+E176+E177+E178) / (B2+B4)) * 100
L4RP	((E155+E166+E167+E168+E179) / (B2+B4)) * 100
MEMP	((E156+E157+E158+E159) / (B2+B4)) * 100
LPARCPU	(((1/CPSP/1,000,000) * B0) / Interval *in Seconds*) * 100

CPI – Cycles per Instruction
Prb State - % Problem State
L1MP – Level 1 Miss Per 100 instructions
L2P – % sourced from Level 2 cache
L3P – % sourced from Level 3 on same Chip cache
L4LP – % sourced from Level 4 Local cache (on same drawer)
L4RP – % sourced from Level 4 Remote cache (on different drawer)
MEMP - % sourced from Memory
LPARCPU - APPL% (GCPs, zIIPs) captured and uncaptured

Workload Characterization
L1 Sourcing from cache/memory hierarchy

B* - Basic Counter Set - Counter Number
P* - Problem-State Counter Set - Counter Number
– See “The Load-Program-Parameter and CPU-Measurement Facilities” SA23-2260 for full description
E* - Extended Counters - Counter Number
– See “IBM The CPU-Measurement Facility Extended Counters Definition for z10, z196/ z114, zEC12 /zBC12, z13/z13s, z14, z15, z16 and z17” SA23-2261-09 for full description
CPSP - SMF113_1_CPSP “CPU Speed”

Formulas – z17 Additional

Updated April 8, 2025

Note these Formulas may change in the future

Metric	**Calculation–** *note all fields are deltas. SMF113-1s are deltas. SMF 113-2s are cumulative.*
Est Instr Cmplx CPI	CPI – Finite CPI
Finite CPI	E143 / B1
SCPL1M	E143 / (B2+B4)
Rel Nest Intensity	4.7x(0.45xL3P+1.2xL4LP+4.5xL4RP+6.0xMEMP)/100
Eff GHz	CPSP / 1000

Est Instr Cmplx CPI – Estimated Instruction Complexity CPI (infinite L1)
Est Finite CPI – Estimated CPI from Finite cache/memory
Est SCPL1M – Estimated Sourcing Cycles per Level 1 Miss
Rel Nest Intensity –Reflects distribution and latency of sourcing from shared caches and memory
Eff GHz – Effective gigahertz for GCPs, cycles per nanosecond

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B* - Basic Counter Set - Counter Number
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CPSP - SMF113_1_CPSP “CPU Speed”

Formulas – z17
Additional TLB

Updated April 8, 2025

Note these Formulas may change in the future

Metric	**Calculation –** *note all fields are deltas. SMF113-1s are deltas. SMF 113-2s are cumulative.*
Est. TLB1 CPU Miss % of Total CPU	((E130+E135) / B0) * (E143 / (B3+B5)) *100
Estimated TLB1 Cycles per TLB Miss	(E130+E135) / (E129+E134) * (E143 / (B3+B5))
PTE % of all TLB1 Misses	N/A with processor design change
TLB Miss Rate	(E129 + E134) / interval

Est. TLB1 CPU Miss % of Total CPU – Estimated TLB CPU % of Total CPU
Estimated TLB1 Cycles per TLB Miss – Estimated Cycles per TLB Miss
PTE % of all TLB1 Misses – Page Table Entry % misses
TLB Miss Rate – TLB Misses per interval (interval is defined by user for length of measurement and units)

B* - Basic Counter Set - Counter Number
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– See “The Load-Program-Parameter and CPU-Measurement Facilities” SA23-2260 for full description
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CPSP - SMF113_1_CPSP “CPU Speed”

Formulas – z17
Additional AIU

Updated April 8, 2025

Note these Formulas may change in the future

Metric	**Calculation –** *note all fields are deltas. SMF113-1s are deltas. SMF 113-2s are cumulative.*
W_AIU_CPU	(((1/CPSP/1,000,000) * E269) / Interval *in Seconds*) * 100
C_AIU_CPU	(((1/CPSP/1,000,000) * E270) / Interval *in Seconds*) * 100
AIU_CPU	W_AIU_CPU + C_AIU_CPU
LOCAL_AIU %	E272 / E267 * 100
REMOTE_AIU %	E273 / E267 * 100
C_AIU_TIME	E270 / E268 * (1 / CPSP)
W_AIU_TIME	E269 / E268 * (1 / CPSP)

Counter definitions

Counter 267 – Increments by one for every NEURAL NETWORK PROCESSING ASSIST (NNPA) instruction executed

Counter 268 – Increments by one for every NEURAL NETWORK PROCESSING ASSIST (NNPA) instruction executed that ended in Condition Code 0

Counter 269 – Cycles CPU spent obtaining access to IBM Z Integrated Accelerator for AI

Counter 270 – Cycles CPU is using IBM Z Integrated Accelerator for AI

Counter 272 – A NEURAL NETWORK PROCESSING ASSIST (NNPA) instruction has used the Local On-Chip IBM Z Integrated Accelerator for AI during its execution

Counter 273 - A NEURAL NETWORK PROCESSING ASSIST (NNPA) instruction has used an Off-Chip IBM Z Integrated Accelerator for AI during its execution

W_AIU_CPU – Waiting for access to AIU (LPARCPU units)
C_AIU_CPU – Executing on AIU (LPARCPU units)
AIU_CPU – Total AIU CPU (LPARCPU units)
LOCAL_AIU % – Percent of NNPA invocations executing on local AIU
REMOTE_AIU % – Percent of NNPA invocations executing on remote AIU
C_AIU_TIME – AVG microseconds executing per completed instruction
W_AIU_TIME – AVG microseconds waiting per completed instruction

B* - Basic Counter Set - Counter Number
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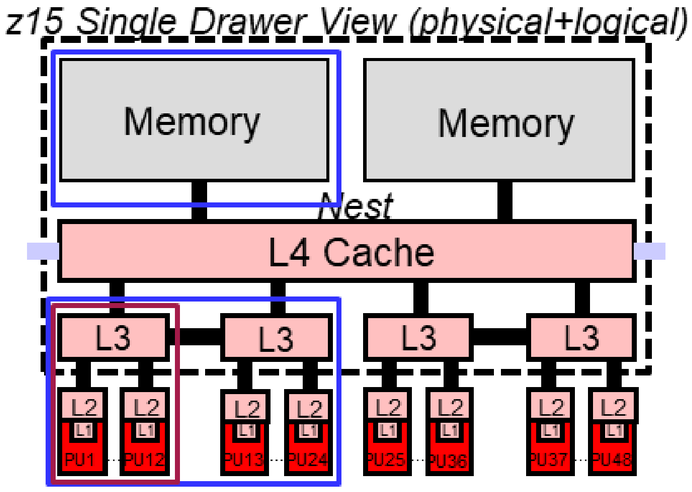
CPSP - SMF113_1_CPSP “CPU Speed”

IBM z16 Metrics

z16 vs z15 Hardware Comparison

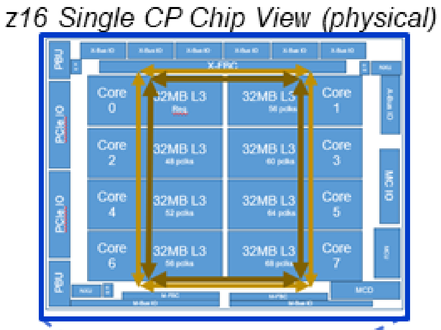
z15 CPU 5.2 GHz
Caches L1 private 128k i, 128k d / core
L2 private 4 MB i, 4 MB d / core
L3 shared 256 MB / CP chip
L4 shared 960 MB / drawer

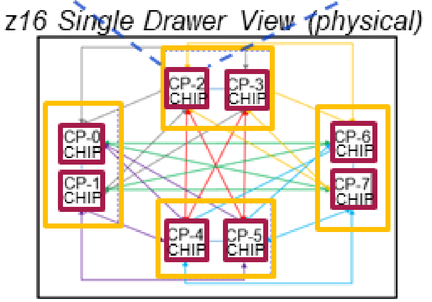
Topology
- 12 cores + 1 L3 / CP chip
- 2 CP chips / cluster
- 2 clusters + 1 L4 (48 engines) / drawer
- 5 drawers / CEC
- Book interconnect: numa star

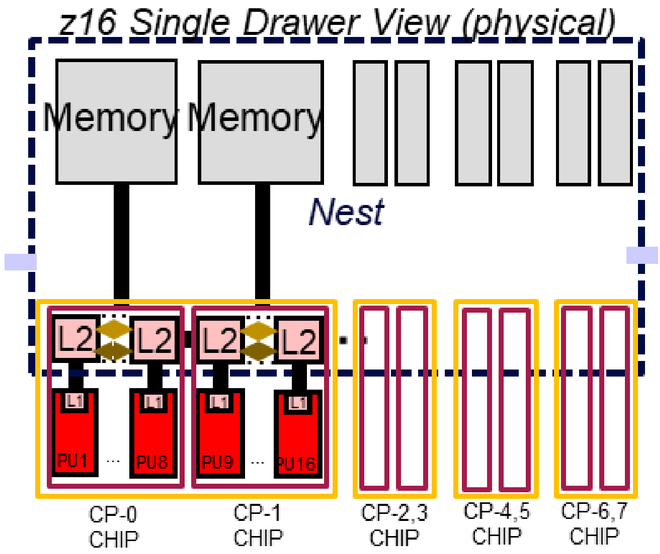


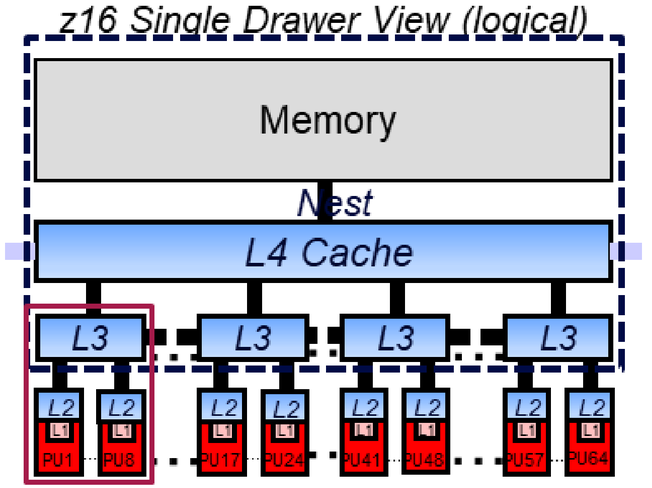
z16 CPU 5.2 GHz
Caches L1 private 128k i, 128k d / core
L2 *private* 32 MB unified / core
virtual victim L3 up to 7x32 = 224 MB / CP chip
virtual victim L4 up to 8x32x7 = 1.75 GB / drawer

Topology
- 8 (core + L3)s / CP chip
- 2 CP chips / DCM
- 4 DCMs (64 engines) / drawer
- 4 drawers / CEC
- Book interconnect: numa star









Formulas – z16

Updated May 31, 2022

Note these Formulas may change in the future

Metric	**Calculation –** *note all fields are deltas. SMF113-1s are deltas. SMF 113-2s are cumulative.*
CPI	B0 / B1
PRBSTATE	(P33 / B1) * 100
L1MP	((B2+B4) / B1) * 100
L2P	((E145+E146+E169+E170) / (B2+B4)) * 100
L3P	((E147+E149+E150+E151+E171+E173+E174+E175) / (B2+B4)) * 100
L4LP	((E148+E152+E153+E154+E160+E161+E162+E163+E164+E165+E172+E176+E177+E178) / (B2+B4)) * 100
L4RP	((E155+E166+E167+E168+E179) / (B2+B4)) * 100
MEMP	((E156+E157+E158+E159+E180+E181+E182+E183) / (B2+B4)) * 100
LPARCPU	(((1/CPSP/1,000,000) * B0) / Interval *in Seconds*) * 100

CPI – Cycles per Instruction
Prb State - % Problem State
L1MP – Level 1 Miss Per 100 instructions
L2P – % sourced from Level 2 cache
L3P – % sourced from Level 3 on same Chip cache
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CPSP - SMF113_1_CPSP “CPU Speed”

Formulas – z16 Additional

Updated June 25, 2024

Note these Formulas may change in the future

Metric	**Calculation–** *note all fields are deltas. SMF113-1s are deltas. SMF 113-2s are cumulative.*
Est Instr Cmplx CPI	CPI – Finite CPI
Finite CPI	E143 / B1
SCPL1M	E143 / (B2+B4)
Rel Nest Intensity	4.1*(0.45*L3P + 1.3*L4LP + 5.0*L4RP + 6.1*MEMP) / 100
Eff GHz	CPSP / 1000

Est Instr Cmplx CPI – Estimated Instruction Complexity CPI (infinite L1)
Est Finite CPI – Estimated CPI from Finite cache/memory
Est SCPL1M – Estimated Sourcing Cycles per Level 1 Miss
Rel Nest Intensity –Reflects distribution and latency of sourcing from shared caches and memory
Eff GHz – Effective gigahertz for GCPs, cycles per nanosecond

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CPSP - SMF113_1_CPSP “CPU Speed”

Formulas – z16
Additional TLB

Updated May 31, 2022

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Metric	**Calculation –** *note all fields are deltas. SMF113-1s are deltas. SMF 113-2s are cumulative.*
Est. TLB1 CPU Miss % of Total CPU	((E130+E135) / B0) * (E143 / (B3+B5)) *100
Estimated TLB1 Cycles per TLB Miss	(E130+E135) / (E129+E134) * (E143 / (B3+B5))
PTE % of all TLB1 Misses	N/A with processor design change
TLB Miss Rate	(E129 + E134) / interval

Est. TLB1 CPU Miss % of Total CPU – Estimated TLB CPU % of Total CPU
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PTE % of all TLB1 Misses – Page Table Entry % misses
TLB Miss Rate – TLB Misses per interval (interval is defined by user for length of measurement and units)

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CPSP - SMF113_1_CPSP “CPU Speed”

Formulas – z16
Additional AIU

Updated Aug 14, 2023

Note these Formulas may change in the future

Metric	**Calculation –** *note all fields are deltas. SMF113-1s are deltas. SMF 113-2s are cumulative.*
W_AIU_CPU	(((1/CPSP/1,000,000) * E269) / Interval *in Seconds*) * 100
C_AIU_CPU	(((1/CPSP/1,000,000) * E270) / Interval *in Seconds*) * 100
AIU_CPU	W_AIU_CPU + C_AIU_CPU

Counter definitions

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Counter 269 – Cycles CPU spent obtaining access to IBM Z Integrated Accelerator for AI

Counter 270 – Cycles CPU is using IBM Z Integrated Accelerator for AI

W_AIU_CPU – Waiting for access to AIU (LPARCPU units)
C_AIU_CPU – Executing AIU (LPARCPU units)
AIU_CPU –Total AIU CPU (LPARCPU units)

B* - Basic Counter Set - Counter Number
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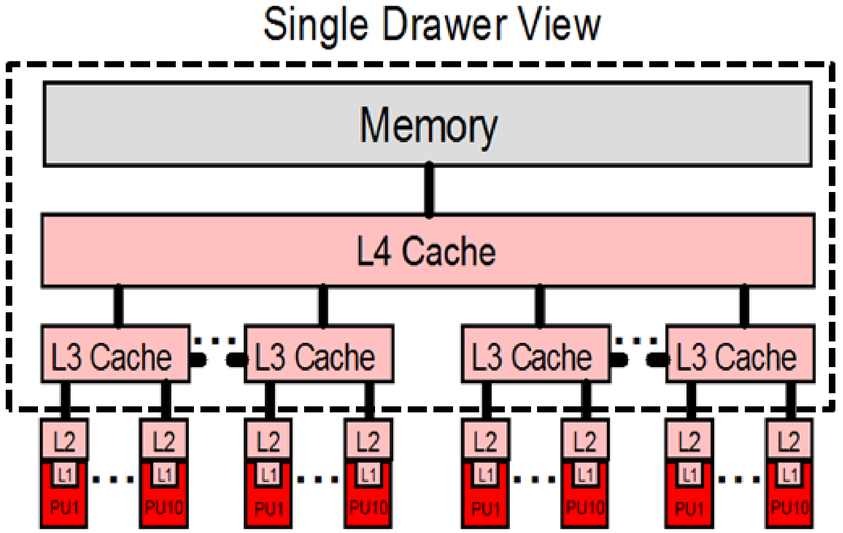
CPSP - SMF113_1_CPSP “CPU Speed”

IBM z15 Metrics

z14 vs z15 Hardware Comparison

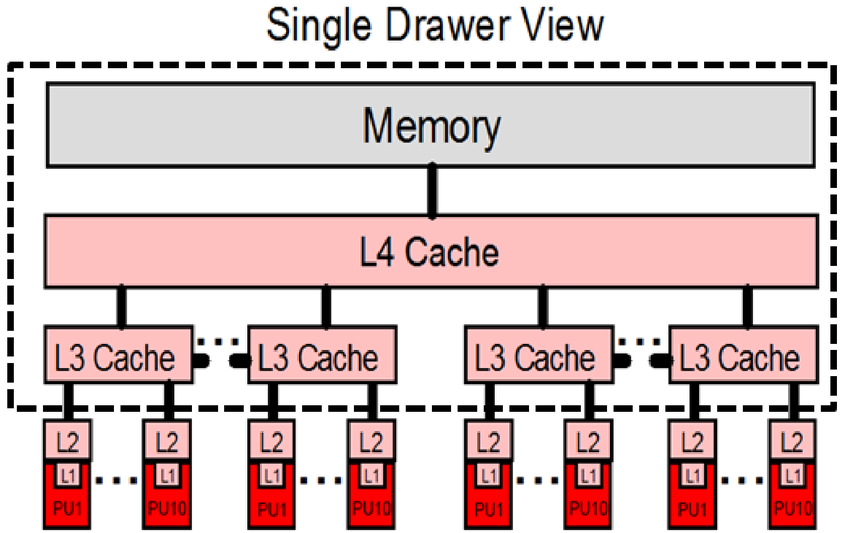
z14 (3906)
– CPU (14nm SOI)
  • 5.2 GHz
– Caches
  • L1 private 128k i, 128k d
  • L2 private 2 MB i, 4 MB d
  • L3 shared 128 MB per chip
  • L4 shared 672 MB per drawer

Topology
– 10 cores + 1 L3 per CP chip
– 2-or-3 CP chips per cluster
– 2 clusters + 1 L4 per drawer
– 4 drawers max per CPC
– Book interconnect: NUMA star



z15 (8561)
– CPU (14 nm SOI)
  • 5.2 GHz
Caches
– L1 private 128k i, 128k d
– L2 private **4 MB i**, 4 MB d
– L3 shared **256 MB** per chip
– L4 shared **960 MB** per drawer

Topology
– **12** cores + 1 L3 per CP chip
– **2** CP chips per cluster
– 2 clusters + 1 L4 per drawer
– **5** drawers max per CPC
– Book interconnect: NUMA star



Formulas – z15

Updated September 23, 2019

Note these Formulas may change in the future

Metric	**Calculation –** *note all fields are deltas. SMF113-1s are deltas. SMF 113-2s are cumulative.*
CPI	B0 / B1
PRBSTATE	(P33 / B1) * 100
L1MP	((B2+B4) / B1) * 100
L2P	((E133+E136) / (B2+B4)) * 100
L3P	((E144+E146+E162+E164) / (B2+B4)) * 100
L4LP	((E147+E149+E156+E165+E167+E174+E150+E152+E158+E168+E170) / (B2+B4)) * 100
L4RP	((E153+E155+E157+E171+E173+E175) / (B2+B4)) * 100
MEMP	((E145 + E148 + E151 + E154 + E163 + E166 + E169 + E172) / (B2+B4)) * 100
LPARCPU	(((1/CPSP/1,000,000) * B0) / Interval *in Seconds*) * 100

CPI – Cycles per Instruction
Prb State - % Problem State
L1MP – Level 1 Miss Per 100 instructions
L2P – % sourced from Level 2 cache
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MEMP - % sourced from Memory
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CPSP - SMF113_1_CPSP “CPU Speed”

Formulas – z15 Additional

Updated December 7, 2023

Note these Formulas may change in the future

Metric	**Calculation–** *note all fields are deltas. SMF113-1s are deltas. SMF 113-2s are cumulative.*
Est Instr Cmplx CPI	CPI – Estimated Finite CPI
Finite CPI	(E143 / B1) + .15
SCPL1M	Estimated Finite CPI / (L1MP / 100)
Rel Nest Intensity	2.9*(0.45*L3P + 1.5*L4LP + 3.2*L4RP + 6.5*MEMP) / 100
Eff GHz	CPSP / 1000

Est Instr Cmplx CPI – Estimated Instruction Complexity CPI (infinite L1)
Est Finite CPI – Estimated CPI from Finite cache/memory
Est SCPL1M – Estimated Sourcing Cycles per Level 1 Miss
Rel Nest Intensity –Reflects distribution and latency of sourcing from shared caches and memory
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CPSP - SMF113_1_CPSP “CPU Speed”

Formulas – z15
Additional TLB

Updated September 23, 2019

Note these Formulas may change in the future

Metric	**Calculation –** *note all fields are deltas. SMF113-1s are deltas. SMF 113-2s are cumulative.*
Est. TLB1 CPU Miss % of Total CPU	((E130+E135) / B0) * (E143 / (B3+B5)) *100
Estimated TLB1 Cycles per TLB Miss	(E130+E135) / (E129+E134) * (E143 / (B3+B5))
PTE % of all TLB1 Misses	N/A with processor design change
TLB Miss Rate	(E129 + E134) / interval

Est. TLB1 CPU Miss % of Total CPU – Estimated TLB CPU % of Total CPU
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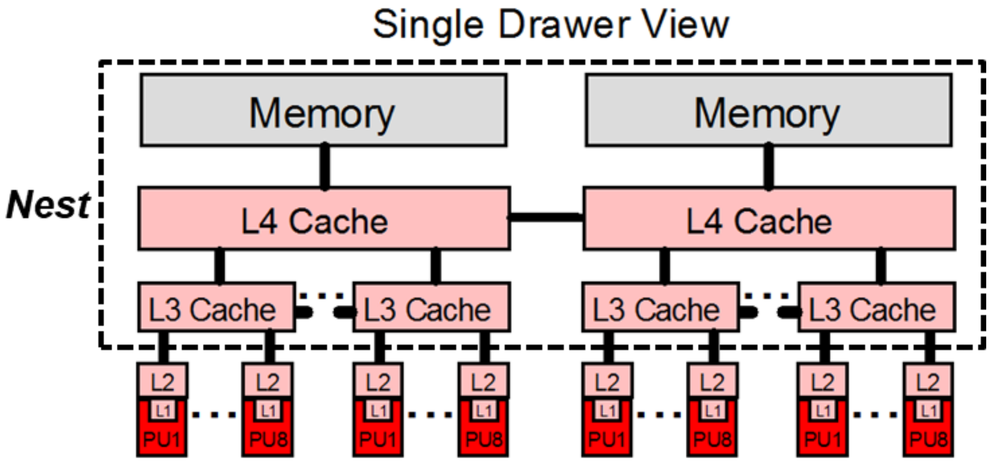
CPSP - SMF113_1_CPSP “CPU Speed”

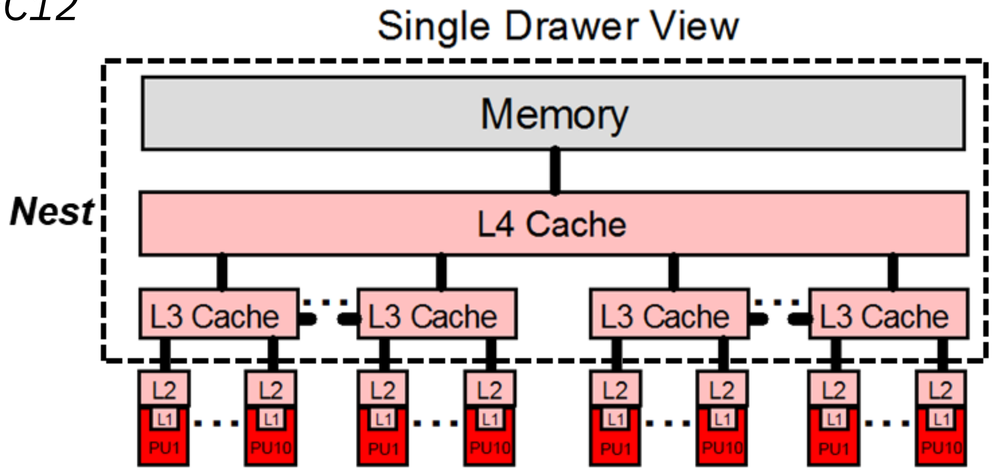
IBM z14 Metrics

z13 vs z14 Hardware Comparison

z13
– CPU
  • 5.0 GHz
  • Major pipeline enhancements
  • 1 picocoded translation engine
– Caches
  • L1 private 96k i, 128k d
  • L2 private 2 MB i, 2 MB d
  • L3 shared 64 MB / chip
  • L4 shared 480 MB / node
    – Plus 224 MB NIC



z14 – *L3 clustering and cache sizes aside, topology strongly resembles zEC12*
– CPU
  • 5.2 GHz
  • Logical directory w/ inclusive TLB
  • 4 HW-implemented translation engines
– Caches
  • L1 private 128k i, 128k d
  • L2 private 2 MB i, 4 MB d
  • L3 shared 128 MB / chip
  • L4 shared 672 MB / ~~node~~ drawer



Formulas – z14

Updated December 2017

Note these Formulas may change in the future

Metric	**Calculation –** *note all fields are deltas. SMF113-1s are deltas. SMF 113-2s are cumulative.*
CPI	B0 / B1
PRBSTATE	(P33 / B1) * 100
L1MP	((B2+B4) / B1) * 100
L2P	((E133+E136) / (B2+B4)) * 100
L3P	((E144+E146+E162+E164) / (B2+B4)) * 100
L4LP	((E147+E149+E156+E165+E167+E174+E150+E152+E158+E168+E170) / (B2+B4)) * 100
L4RP	((E153+E155+E157+E171+E173+E175) / (B2+B4)) * 100
MEMP	((E145 + E148 + E151 + E154 + E163 + E166 + E169 + E172) / (B2+B4)) * 100
LPARCPU	(((1/CPSP/1,000,000) * B0) / Interval *in Seconds*) * 100

CPI – Cycles per Instruction
Prb State - % Problem State
L1MP – Level 1 Miss Per 100 instructions
L2P – % sourced from Level 2 cache
L3P – % sourced from Level 3 on same Chip cache
L4LP – % sourced from Level 4 Local cache (on same drawer)
L4RP – % sourced from Level 4 Remote cache (on different drawer)
MEMP - % sourced from Memory
LPARCPU - APPL% (GCPs, zIIPs) captured and uncaptured

Workload Characterization
L1 Sourcing from cache/memory hierarchy

B* - Basic Counter Set - Counter Number
P* - Problem-State Counter Set - Counter Number
– See “The Load-Program-Parameter and CPU-Measurement Facilities” SA23-2260 for full description
E* - Extended Counters - Counter Number
– See “IBM The CPU-Measurement Facility Extended Counters Definition for z10, z196/ z114, zEC12 /zBC12, z13/z13s, z14, z15, z16 and z17” SA23-2261-09 for full description
CPSP - SMF113_1_CPSP “CPU Speed”

Formulas – z14 Additional

Updated December 7, 2023

Note these Formulas may change in the future

Metric	**Calculation–** *note all fields are deltas. SMF113-1s are deltas. SMF 113-2s are cumulative.*
Est Instr Cmplx CPI	CPI – Estimated Finite CPI
Finite CPI	(E143 / B1) + .18
SCPL1M	Estimated Finite CPI / (L1MP / 100)
Rel Nest Intensity	2.4*(0.4*L3P + 1.5*L4LP + 3.2*L4RP + 7.0*MEMP) / 100
Eff GHz	CPSP / 1000

Est Instr Cmplx CPI – Estimated Instruction Complexity CPI (infinite L1)
Est Finite CPI – Estimated CPI from Finite cache/memory
Est SCPL1M – Estimated Sourcing Cycles per Level 1 Miss
Rel Nest Intensity –Reflects distribution and latency of sourcing from shared caches and memory
Eff GHz – Effective gigahertz for GCPs, cycles per nanosecond

Workload Characterization
L1 Sourcing from cache/memory hierarchy

B* - Basic Counter Set - Counter Number
P* - Problem-State Counter Set - Counter Number
– See “The Load-Program-Parameter and CPU-Measurement Facilities” SA23-2260 for full description
E* - Extended Counters - Counter Number
– See “IBM The CPU-Measurement Facility Extended Counters Definition for z10, z196/ z114, zEC12 /zBC12, z13/z13s, z14, z15, z16 and z17” SA23-2261-09 for full description
CPSP - SMF113_1_CPSP “CPU Speed”

Formulas – z14
Additional TLB

Updated September 23, 2019

Note these Formulas may change in the future

Metric	**Calculation –** *note all fields are deltas. SMF113-1s are deltas. SMF 113-2s are cumulative.*
Est. TLB1 CPU Miss % of Total CPU	((E130+E135) / B0) * (E143 / (B3+B5)) *100
Estimated TLB1 Cycles per TLB Miss	(E130+E135) / (E129+E134) * (E143 / (B3+B5))
PTE % of all TLB1 Misses	N/A with processor design change
TLB Miss Rate	(E129 + E134) / interval

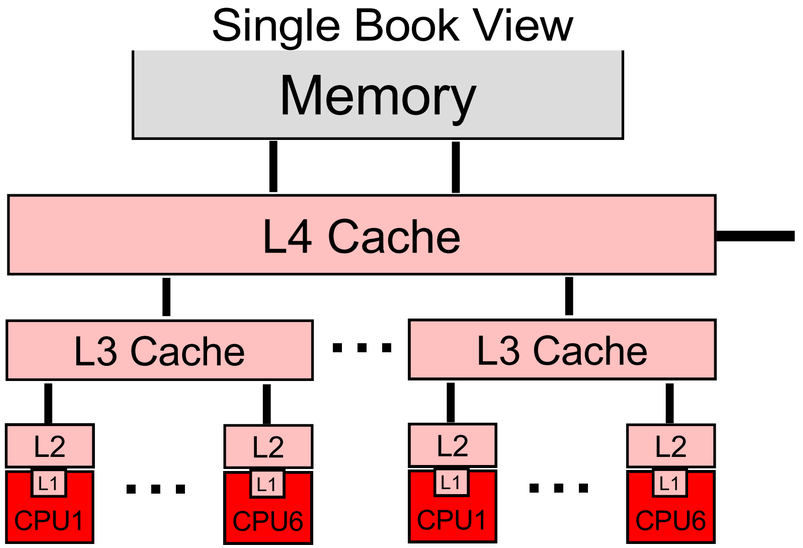
Est. TLB1 CPU Miss % of Total CPU – Estimated TLB CPU % of Total CPU
Estimated TLB1 Cycles per TLB Miss – Estimated Cycles per TLB Miss
PTE % of all TLB1 Misses – Page Table Entry % misses
TLB Miss Rate – TLB Misses per interval (interval is defined by user for length of measurement and units)

B* - Basic Counter Set - Counter Number
P* - Problem-State Counter Set - Counter Number
– See “The Load-Program-Parameter and CPU-Measurement Facilities” SA23-2260 for full description
E* - Extended Counters - Counter Number
– See “IBM The CPU-Measurement Facility Extended Counters Definition for z10, z196/ z114, zEC12 /zBC12, z13/z13s, z14, z15, z16 and z17” SA23-2261-09 for full description
CPSP - SMF113_1_CPSP “CPU Speed”

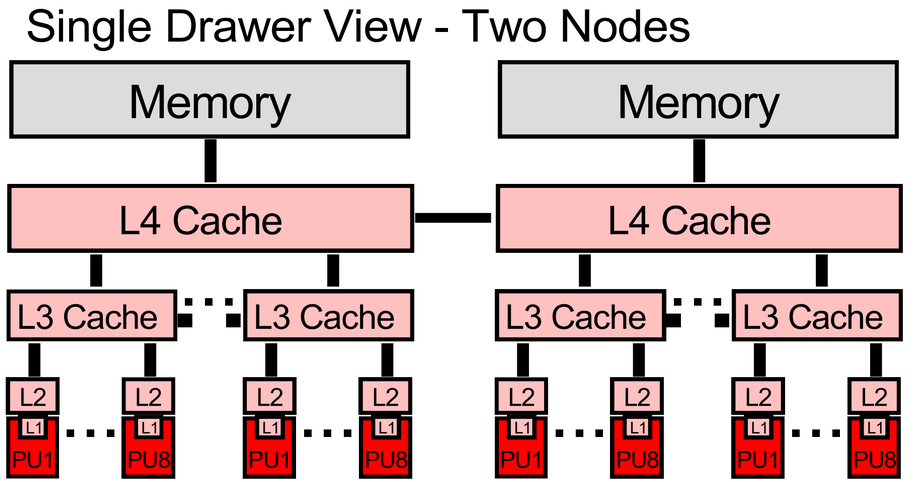
IBM z13 Metrics

z13 vs zEC12 Hardware Comparison

zEC12
– CPU
  • 5.5 GHz
  • Enhanced Out-Of-Order
– Caches
  • L1 private 64k i, 96k d
  • L2 private 1 MB i, 1 MB d
  • L3 shared 48 MB / chip
  • L4 shared 384 MB / node
    – Plus 224 MB NIC



z13
– CPU
  • 5.0 GHz
  • Major pipeline enhancements
– Caches
  • L1 private 96k i, 128k d
  • L2 private 2 MB i, 2 MB d
  • L3 shared 64 MB / chip
  • L4 shared 480 MB / node
    – Plus 224 MB L3 NIC Directory



Formulas – z13

Note these Formulas may change in the future

Metric	**Calculation –** *note all fields are deltas. SMF113-1s are deltas. SMF 113-2s are cumulative.*
CPI	B0 / B1
PRBSTATE	(P33 / B1) * 100
L1MP	((B2+B4) / B1) * 100
L2P	((E133+E136) / (B2+B4)) * 100
L3P	((E144+E145+ E162+E163) / (B2+B4)) * 100
L4LP	((E146+E147+E148+E164+E165+E166) / (B2+B4)) * 100
L4RP	((E149+E150+E151+E152+E153+E154+E155+E156+E157+E167+ E168+E169+E170+E171+E172+ E173+E174+E175) / (B2+B4)) * 100
MEMP	((E158 + E159 + E160 + E161 + E176 + E177 + E178 + E179) / (B2+B4)) * 100
LPARCPU	(((1/CPSP/1,000,000) * B0) / Interval *in Seconds*) * 100

CPI – Cycles per Instruction
Prb State - % Problem State
L1MP – Level 1 Miss Per 100 instructions
L2P – % sourced from Level 2 cache
L3P – % sourced from Level 3 on same Chip cache
L4LP – % sourced from Level 4 Local cache (on same drawer)
L4RP – % sourced from Level 4 Remote cache (on different drawer)
MEMP - % sourced from Memory
LPARCPU - APPL% (GCPs, zIIPs) captured and uncaptured

Workload Characterization
L1 Sourcing from cache/memory hierarchy

B* - Basic Counter Set - Counter Number
P* - Problem-State Counter Set - Counter Number
– See “The Load-Program-Parameter and CPU-Measurement Facilities” SA23-2260 for full description
E* - Extended Counters - Counter Number
– See “IBM The CPU-Measurement Facility Extended Counters Definition for z10, z196/ z114, zEC12 /zBC12, z13/z13s, z14, z15, z16 and z17” SA23-2261-09 for full description
CPSP - SMF113_1_CPSP “CPU Speed”

Formulas – z13 Additional

Updated February 2017

Note these Formulas may change in the future

Metric	**Calculation–** *note all fields are deltas. SMF113-1s are deltas. SMF 113-2s are cumulative.*
Est Instr Cmplx CPI	CPI – Estimated Finite CPI
Finite CPI	E143 / B1
SCPL1M	E143 / (B2+B4)
Rel Nest Intensity	2.3*(0.4*L3P + 1.6*L4LP + 3.5*L4RP + 7.5*MEMP) / 100
Eff GHz	CPSP / 1000

Est Instr Cmplx CPI – Estimated Instruction Complexity CPI (infinite L1)
Est Finite CPI – Estimated CPI from Finite cache/memory
Est SCPL1M – Estimated Sourcing Cycles per Level 1 Miss
Rel Nest Intensity –Reflects distribution and latency of sourcing from shared caches and memory
Eff GHz – Effective gigahertz for GCPs, cycles per nanosecond

Workload Characterization
L1 Sourcing from cache/memory hierarchy

B* - Basic Counter Set - Counter Number
P* - Problem-State Counter Set - Counter Number
– See “The Load-Program-Parameter and CPU-Measurement Facilities” SA23-2260 for full description
E* - Extended Counters - Counter Number
– See “IBM The CPU-Measurement Facility Extended Counters Definition for z10, z196/ z114, zEC12 /zBC12, z13/z13s, z14, z15, z16 and z17” SA23-2261-09 for full description
CPSP - SMF113_1_CPSP “CPU Speed”

Formulas – z13 / z13s
Additional TLB

Note these Formulas may change in the future

Metric	**Calculation –** *note all fields are deltas. SMF113-1s are deltas. SMF 113-2s are cumulative.*
Est. TLB1 CPU Miss % of Total CPU	((E130+E135) / B0) * (E143 / (B3+B5)) *100
Estimated TLB1 Cycles per TLB Miss	(E130+E135) / (E129+E134) * (E143 / (B3+B5))
PTE % of all TLB1 Misses	(E137 / (E129+E134)) * 100
TLB Miss Rate	(E129 + E134) / interval

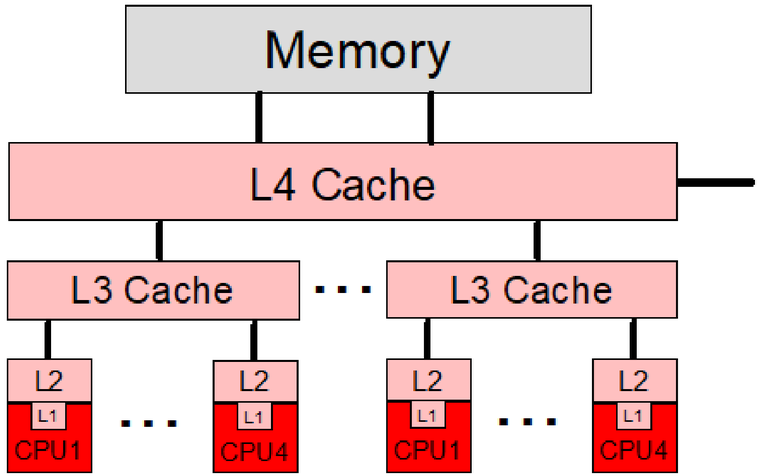
Est. TLB1 CPU Miss % of Total CPU – Estimated TLB CPU % of Total CPU
Estimated TLB1 Cycles per TLB Miss – Estimated Cycles per TLB Miss
PTE % of all TLB1 Misses – Page Table Entry % misses
TLB Miss Rate – TLB Misses per interval (interval is defined by user for length of measurement and units)

B* - Basic Counter Set - Counter Number
P* - Problem-State Counter Set - Counter Number
– See “The Load-Program-Parameter and CPU-Measurement Facilities” SA23-2260 for full description
E* - Extended Counters - Counter Number
– See “IBM The CPU-Measurement Facility Extended Counters Definition for z10, z196/ z114, zEC12 /zBC12, z13/z13s, z14, z15, z16 and z17” SA23-2261-09 for full description
CPSP - SMF113_1_CPSP “CPU Speed”

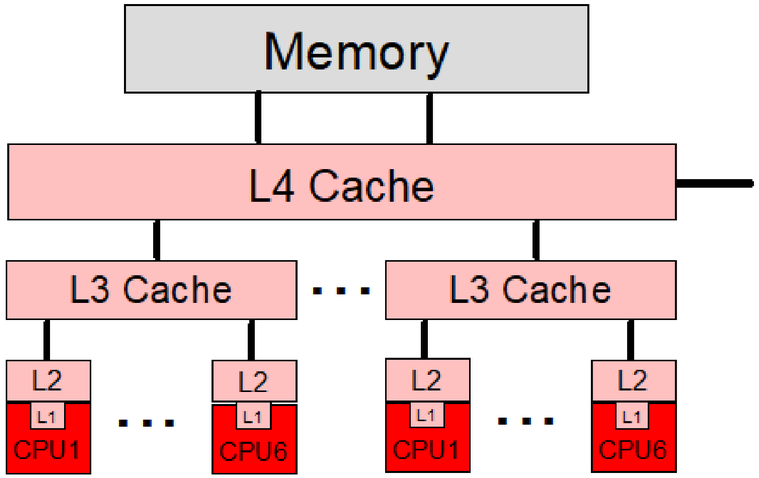
IBM zEC12 Metrics

zEC12 vs z196 Hardware Comparison

z196
– CPU
  • 5.2 GHz
  • Out-Of-Order execution
– Caches
  • L1 private 64k i, 128k d
  • L2 private 1.5 MB
  • L3 shared 24 MB / chip
  • L4 shared 192 MB / book



zEC12
– CPU
  • 5.5 GHz
  • Enhanced Out-Of-Order
– Caches
  • L1 private 64k i, 96k d
  • L2 private 1 MB I + 1 MB d
  • L3 shared 48 MB / chip
  • L4 shared 385 MB / book



Formulas – zEC12 / zBC12

Note these Formulas may change in the future

Metric	**Calculation –** *note all fields are deltas. SMF113-1s are deltas. SMF 113-2s are cumulative.*
CPI	B0 / B1
PRBSTATE	(P33 / B1) * 100
L1MP	((B2+B4) / B1) * 100
L2P	((E130+E131+E132) / (B2+B4)) * 100
L3P	((E144+E150+E153+E159) / (B2+B4)) * 100
L4LP	((E147+E145+E151+E156+E154+E160) / (B2+B4)) * 100
L4RP	((E148+E146+E152+E157+E155+E161) / (B2+B4)) * 100
MEMP	(((E135+E137) + (B2+B4-E130-E131-E132-E144-E150-E153-E159-E147-E145-E151-E156-E154-E160-E148-E146-E152-E157-E155-E161-E135-E137)) / (B2+B4)) * 100
LPARCPU	(((1/CPSP/1,000,000) * B0) / Interval *in Seconds*) * 100

CPI – Cycles per Instruction
Prb State - % Problem State
L1MP – Level 1 Miss Per 100 instructions
L2P – % sourced from Level 2 cache
L3P – % sourced from Level 3 on same Chip cache
L4LP – % sourced from Level 4 Local cache (on same drawer)
L4RP – % sourced from Level 4 Remote cache (on different drawer)
MEMP - % sourced from Memory
LPARCPU - APPL% (GCPs, zIIPs) captured and uncaptured

Workload Characterization
L1 Sourcing from cache/memory hierarchy

B* - Basic Counter Set - Counter Number
P* - Problem-State Counter Set - Counter Number
– See “The Load-Program-Parameter and CPU-Measurement Facilities” SA23-2260 for full description
E* - Extended Counters - Counter Number
– See “IBM The CPU-Measurement Facility Extended Counters Definition for z10, z196/ z114, zEC12 /zBC12, z13/z13s, z14, z15, z16 and z17” SA23-2261-09 for full description
CPSP - SMF113_1_CPSP “CPU Speed”

Formulas – zEC12 / zBC12 Additional

Updated January 2015
Note these Formulas may change in the future

Metric	**Calculation–** *note all fields are deltas. SMF113-1s are deltas. SMF 113-2s are cumulative.*
Est Instr Cmplx CPI	CPI – Estimated Finite CPI
Finite CPI	((B3+B5) / B1) * (.54 + (0.04*RNI))
SCPL1M	((B3+B5) / (B2+B4)) * (.54 + (0.04*RNI))
Rel Nest Intensity	2.3*(0.4*L3P + 1.2*L4LP + 2.7*L4RP + 8.2*MEMP) / 100
Eff GHz	CPSP / 1000

Est Instr Cmplx CPI – Estimated Instruction Complexity CPI (infinite L1)
Est Finite CPI – Estimated CPI from Finite cache/memory
Est SCPL1M – Estimated Sourcing Cycles per Level 1 Miss
Rel Nest Intensity –Reflects distribution and latency of sourcing from shared caches and memory
Eff GHz – Effective gigahertz for GCPs, cycles per nanosecond

Workload Characterization
L1 Sourcing from cache/memory hierarchy

B* - Basic Counter Set - Counter Number
P* - Problem-State Counter Set - Counter Number
– See “The Load-Program-Parameter and CPU-Measurement Facilities” SA23-2260 for full description
E* - Extended Counters - Counter Number
– See “IBM The CPU-Measurement Facility Extended Counters Definition for z10, z196/ z114, zEC12 /zBC12, z13/z13s, z14, z15, z16 and z17” SA23-2261-09 for full description
CPSP - SMF113_1_CPSP “CPU Speed”

Formulas – zEC12 / zBC12
Additional TLB

Note these Formulas may change in the future

Metric	**Calculation –** *note all fields are deltas. SMF113-1s are deltas. SMF 113-2s are cumulative.*
Est. TLB1 CPU Miss % of Total CPU	((E128+E129) / B0) * 100 * .65
Estimated TLB1 Cycles per TLB Miss	(E128+E129) / (E133+E140) * .65
PTE % of all TLB1 Misses	(E141 / (E133+E140)) * 100

Est. TLB1 CPU Miss % of Total CPU – Estimated TLB CPU % of Total CPU
Estimated TLB1 Cycles per TLB Miss – Estimated Cycles per TLB Miss
PTE % of all TLB1 Misses – Page Table Entry % misses
TLB Miss Rate – TLB Misses per interval (interval is defined by user for length of measurement and units)

B* - Basic Counter Set - Counter Number
P* - Problem-State Counter Set - Counter Number
– See “The Load-Program-Parameter and CPU-Measurement Facilities” SA23-2260 for full description
E* - Extended Counters - Counter Number
– See “IBM The CPU-Measurement Facility Extended Counters Definition for z10, z196/ z114, zEC12 /zBC12, z13/z13s, z14, z15, z16 and z17” SA23-2261-09 for full description
CPSP - SMF113_1_CPSP “CPU Speed”

IBM z10 and z196 Metrics

Formulas – z196

Note these Formulas may change in the future

Metric	**Calculation –** *note all fields are deltas. SMF113-1s are deltas. SMF 113-2s are cumulative.*
CPI	B0 / B1
PRBSTATE	(P33 / B1) * 100
L1MP	((B2+B4) / B1) * 100
L2P	((E128+E129) / (B2+B4)) * 100
L3P	((E150+E153) / (B2+B4)) * 100
L4LP	((E135+E136+E152+E155) / (B2+B4)) * 100
L4RP	((E138+E139+E134+E143) / (B2+B4)) * 100
MEMP	(((E141+E142) + (B2+B4-E128-E129-E150-E153-E135-E136-E152-E155-E138-E139-E134-E143-E141-E142)) / (B2+B4)) * 100
LPARCPU	(((1/CPSP/1,000,000) * B0) / Interval *in Seconds*) * 100

CPI – Cycles per Instruction
Prb State - % Problem State
L1MP – Level 1 Miss Per 100 instructions
L2P – % sourced from Level 2 cache
L3P – % sourced from Level 3 on same Chip cache
L4LP – % sourced from Level 4 Local cache (on same drawer)
L4RP – % sourced from Level 4 Remote cache (on different drawer)
MEMP - % sourced from Memory
LPARCPU - APPL% (GCPs, zIIPs) captured and uncaptured

Workload Characterization
L1 Sourcing from cache/memory hierarchy

B* - Basic Counter Set - Counter Number
P* - Problem-State Counter Set - Counter Number
– See “The Load-Program-Parameter and CPU-Measurement Facilities” SA23-2260 for full description
E* - Extended Counters - Counter Number
– See “IBM The CPU-Measurement Facility Extended Counters Definition for z10, z196/ z114, zEC12 /zBC12, z13/z13s, z14, z15, z16 and z17” SA23-2261-09 for full description
CPSP - SMF113_1_CPSP “CPU Speed”

Formulas – z196 Additional

Updated July 2012

Note these Formulas may change in the future

Metric	**Calculation–** *note all fields are deltas. SMF113-1s are deltas. SMF 113-2s are cumulative.*
Est Instr Cmplx CPI	CPI – Estimated Finite CPI
Finite CPI	((B3+B5) / B1) * (.59 + (0.1*RNI))
SCPL1M	((B3+B5) / (B2+B4)) * (.59 + (0.1*RNI))
Rel Nest Intensity	1.67*(0.4*L3P + 1.0*L4LP + 2.4*L4RP + 7.5*MEMP) / 100
Eff GHz	CPSP / 1000

Est Instr Cmplx CPI – Estimated Instruction Complexity CPI (infinite L1)
Est Finite CPI – Estimated CPI from Finite cache/memory
Est SCPL1M – Estimated Sourcing Cycles per Level 1 Miss
Rel Nest Intensity –Reflects distribution and latency of sourcing from shared caches and memory
Eff GHz – Effective gigahertz for GCPs, cycles per nanosecond

Workload Characterization
L1 Sourcing from cache/memory hierarchy

B* - Basic Counter Set - Counter Number
P* - Problem-State Counter Set - Counter Number
– See “The Load-Program-Parameter and CPU-Measurement Facilities” SA23-2260 for full description
E* - Extended Counters - Counter Number
– See “IBM The CPU-Measurement Facility Extended Counters Definition for z10, z196/ z114, zEC12 /zBC12, z13/z13s, z14, z15, z16 and z17” SA23-2261-09 for full description
CPSP - SMF113_1_CPSP “CPU Speed”

Formulas – z196
Additional TLB

Updated August 2012

Note these Formulas may change in the future

Metric	**Calculation –** *note all fields are deltas. SMF113-1s are deltas. SMF 113-2s are cumulative.*
Est. TLB1 CPU Miss % of Total CPU	((E130+E131) / B0) * 100 * .61
Estimated TLB1 Cycles per TLB Miss	(E130+E131) / (E144+E145) * .61
PTE % of all TLB1 Misses	(E146 / (E144+E145)) * 100

Est. TLB1 CPU Miss % of Total CPU – Estimated TLB CPU % of Total CPU
Estimated TLB1 Cycles per TLB Miss – Estimated Cycles per TLB Miss
PTE % of all TLB1 Misses – Page Table Entry % misses
TLB Miss Rate – TLB Misses per interval (interval is defined by user for length of measurement and units)

B* - Basic Counter Set - Counter Number
P* - Problem-State Counter Set - Counter Number
– See “The Load-Program-Parameter and CPU-Measurement Facilities” SA23-2260 for full description
E* - Extended Counters - Counter Number
– See “IBM The CPU-Measurement Facility Extended Counters Definition for z10, z196/ z114, zEC12 /zBC12, z13/z13s, z14, z15, z16 and z17” SA23-2261-09 for full description
CPSP - SMF113_1_CPSP “CPU Speed”

Formulas – z10

Note these Formulas may change in the future

Metric	**Calculation –** *note all fields are deltas. SMF113-1s are deltas. SMF 113-2s are cumulative.*
CPI	B0 / B1
PRBSTATE	(P33 / B1) * 100
L1MP	((B2+B4) / B1) * 100
L2P	((E128+E129) / (B2+B4)) * 100
L3P	((E130+E131) / (B2+B4)) * 100
L4LP	((E132+E133) / (B2+B4)) * 100
L4RP	(((E134+E135) + (B2+B4-E128-E129-E130-E131-E132-E133-E134-E135)) / (B2+B4)) * 100
MEMP	(((1/CPSP/1,000,000) * B0) / Interval *in Seconds*) * 100
LPARCPU	B0 / B1

CPI – Cycles per Instruction
Prb State - % Problem State
L1MP – Level 1 Miss Per 100 instructions
L2P – % sourced from Level 2 cache
L3P – % sourced from Level 3 on same Chip cache
L4LP – % sourced from Level 4 Local cache (on same drawer)
L4RP – % sourced from Level 4 Remote cache (on different drawer)
MEMP - % sourced from Memory
LPARCPU - APPL% (GCPs, zIIPs) captured and uncaptured

Workload Characterization
L1 Sourcing from cache/memory hierarchy

B* - Basic Counter Set - Counter Number
P* - Problem-State Counter Set - Counter Number
– See “The Load-Program-Parameter and CPU-Measurement Facilities” SA23-2260 for full description
E* - Extended Counters - Counter Number
– See “IBM The CPU-Measurement Facility Extended Counters Definition for z10, z196/ z114, zEC12 /zBC12, z13/z13s, z14, z15, z16 and z17” SA23-2261-09 for full description
CPSP - SMF113_1_CPSP “CPU Speed”

Formulas – z10 Additional

Note these Formulas may change in the future

Metric	**Calculation–** *note all fields are deltas. SMF113-1s are deltas. SMF 113-2s are cumulative.*
Est Instr Cmplx CPI	CPI – Estimated Finite CPI
Finite CPI	((B3+B5) / B1) * .84
SCPL1M	((B3+B5) / (B2+B4)) * .84
Rel Nest Intensity	(1.0*L2LP + 2.4*L2RP + 7.5*MEMP) / 100
Eff GHz	CPSP / 1000

Est Instr Cmplx CPI – Estimated Instruction Complexity CPI (infinite L1)
Est Finite CPI – Estimated CPI from Finite cache/memory
Est SCPL1M – Estimated Sourcing Cycles per Level 1 Miss
Rel Nest Intensity –Reflects distribution and latency of sourcing from shared caches and memory
Eff GHz – Effective gigahertz for GCPs, cycles per nanosecond

Workload Characterization
L1 Sourcing from cache/memory hierarchy

B* - Basic Counter Set - Counter Number
P* - Problem-State Counter Set - Counter Number
– See “The Load-Program-Parameter and CPU-Measurement Facilities” SA23-2260 for full description
E* - Extended Counters - Counter Number
– See “IBM The CPU-Measurement Facility Extended Counters Definition for z10, z196/ z114, zEC12 /zBC12, z13/z13s, z14, z15, z16 and z17” SA23-2261-09 for full description
CPSP - SMF113_1_CPSP “CPU Speed”

Formulas – z10
Additional TLB

Updated March 2012
Note these Formulas may change in the future

Metric	**Calculation –** *note all fields are deltas. SMF113-1s are deltas. SMF 113-2s are cumulative.*
Est. TLB1 CPU Miss % of Total CPU	((E145+E146) / B0) * 100 * .31
Estimated TLB1 Cycles per TLB Miss	(E145+E146) / (E138+E139) * .31
PTE % of all TLB1 Misses	(E140 / (E138+E139)) * 100

Est. TLB1 CPU Miss % of Total CPU – Estimated TLB CPU % of Total CPU
Estimated TLB1 Cycles per TLB Miss – Estimated Cycles per TLB Miss
PTE % of all TLB1 Misses – Page Table Entry % misses

B* - Basic Counter Set - Counter Number
P* - Problem-State Counter Set - Counter Number
– See “The Load-Program-Parameter and CPU-Measurement Facilities” SA23-2260 for full description
E* - Extended Counters - Counter Number
– See “IBM The CPU-Measurement Facility Extended Counters Definition for z10, z196/ z114, zEC12 /zBC12, z13/z13s, z14, z15, z16 and z17” SA23-2261-09 for full description
CPSP - SMF113_1_CPSP “CPU Speed”

Definitions

CPI
– Cycles per Instruction
PRB STATE
– % Problem State
L1MP
– Level 1 Miss Per 100 instructions
L15P / L2P
– % sourced from L1.5 or L2 cache
L2LP
– % sourced from Level 2 (or L4) Local cache
– on same book or drawer
L2RP
– % sourced from Level 2 (or L4) Remote cache
– From different book or drawer
L3P
– % sourced from L3 cache
MEMP
– % sourced from Memory

LPARCPU
– APPL% (GCPs, zAAPs, zIIPs) captured and uncaptured
Est Instr Cmplx CPI
– Estimated Instruction Complexity CPI
Est Finite CPI
– Estimated Finite CPI
Est SCPL1M
– Estimated Sourcing Cycles per L1 Miss Per 100 instructions
Rel Nest Intensity
– Relative Nest Intensity
Eff GHz
– Effective Gigahertz
Machine Type
– Machine Type (e.g. z14, z15, z16, z17)
LSPR Wkld
– LSPR Workload match based on L1MP and RNI

Pool – 1 = GCP, 3 = zAAP, 6 = zIIP

Thank you